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Theodore Van Duzer

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University of California - Berkeley
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The views, opinions and/or findings contained in this report are those of the author(s) and should not contrued as an official Department of the Army position, policy or decision, unless so designated by other documentation.

14. ABSTRACT

The research under this grant is a part of the realization of a hybrid Josephson-CMOS memory which will operate at 4 K and will provide the random access memory needed for digital computation by the ultra-high speed superconducting logic circuits. Standard CMOS circuits work about 40% faster at 4 K than at room temperature and are far denser than superconducting circuits so a large amount of memory can be made available. During this grant period, we have designed a CMOS memory by professional standards. We have focused on the key task of

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4 K hybrid memory, Hybrid Josephson-CMOS memory

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a. REPORT	b. ABSTRACT	c. THIS PAGE			Theodore Van Duzer
UU	UU	UU	UU		19b. TELEPHONE NUMBER: 510-642-3306

Report Title

Final Technical Report, "Novel Memory Structure for 4 K operation with Interfacing to Josephson Digital Circuits"

ABSTRACT

The research under this grant is a part of the realization of a hybrid Josephson-CMOS memory which will operate at 4 K and will provide the random access memory needed for digital computation by the ultra-high speed superconducting logic circuits. Standard CMOS circuits work about 40% faster at 4 K than at room temperature and are far denser than superconducting circuits so a large amount of memory can be made available. During this grant period, we have designed a CMOS memory by professional standards. We have focused on the key task of amplifying the Josephson millivolt signals to volt level as required by the CMOS memory. In particular, we have designed a sensitive CMOS amplifier with the appropriate Josephson preamplifier. Testing during this period has revealed that the almost infinite charge retention time observed in 350 nm CMOS devices does not appear in 180 nm devices due to leakage; this has led to extensive reconsiderations in our design. In the next design we will use standard SRAM cells which can function independent of leakage. We will also used a biasing circuit which is not degraded by leakage.

List of papers submitted or published that acknowledge ARO support during this reporting period. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

K. Fujiwara, Q. Liu, T. Van Duzer, X. Meng, N. Yoshikawa, "New Delay-Time Measurements on a 64-kb Josepshson-CMOS Hybrid Memory with a 600 ps Access Time", IEEE Trans. Appl. Supercond., Vol. 20, pp. 14-20, Feb. 2010.

Number of Papers published in peer-reviewed journals: 1.00

(b) Papers published in non-peer-reviewed journals or in conference proceedings (N/A for none)

Number of Papers published in non peer-reviewed journals: 0.00

(c) Presentations

Number of Presentations: 0.00

Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts): 0

Peer-Reviewed Conference Proceeding publications (other than abstracts):

Number of Peer-Reviewed Conference Proceeding publications (other than abstracts): 0

(d) Manuscripts

Number of Manuscripts: 0.00

Patents Submitted

Patents Awarded

Graduate Students

NAME	PERCENT_SUPPORTED
Daniel Wei	0.61
FTE Equivalent:	**0.61**
Total Number:	**1**

Names of Post Doctorates

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Names of Faculty Supported

NAME	PERCENT_SUPPORTED	National Academy Member
Theodore Van Duzer	0.25	No
FTE Equivalent:	**0.25**	
Total Number:	**1**	

Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period:	0.00
The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:.....	0.00
The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:.....	0.00
Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):	0.00
Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering:	0.00
The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense	0.00
The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields:	0.00

Names of Personnel receiving masters degrees

NAME
Total Number:

Names of personnel receiving PHDs

NAME
Total Number:

Names of other research staff

NAME	PERCENT SUPPORTED	
Xiao-Fan Meng	0.50	No
Hee Joung Park	1.00	No
Stephen Whiteley	0.10	No
Hongfei Ye	1.00	No
FTE Equivalent:	**2.60**	
Total Number:	**4**	

Sub Contractors (DD882)

Inventions (DD882)

Novel Memory Structure for 4 K Operation with Interfacing to Josephson Digital Circuits

List of illustrations

Statement of the problem studied

Superconducting logic circuits have been shown to function successfully at frequencies much higher than comparable semiconductor circuits and therefore offer an opportunity for faster computers. However, such computers will need random access memory. Earlier work in this field has focused on using circulating currents in superconducting loops as the storage elements. The earliest work was reported in 1969 at IBM [1]. A complete 1-kbit memory with decoding and driving circuits was made. The difficulty of extending it to memories with larger capacity became clear and was an important part of the decision to terminate the entire IBM superconducting computer project in 1983. Other circulating-current memory cells were developed in projects in Japan during the 1980s and complete memories were made. A project at NEC developed a fully functional 4-kbit memory, which was reported in 1999 [2]. This is the largest successful memory based on circulating current memory cells in the literature, although some attempts at 16-kbit memories have been reported. By their nature, memories employ large numbers of junctions and long lines for accessing the cells. The addressing circuits are clocked at gigahertz frequencies and for practical reasons constitute an increasingly challenging design problem for memories with larger capacities. Component statistical spreads, including junction critical currents, inductances, and resistances become increasingly limiting as the number of components increases. An added problem for circulating-current memory cells is ambient magnetic flux and flux due to large supply currents, both of which can cause malfunctions of memory cells that function by storing magnetic flux.

Our approach to providing memory uses a CMOS memory which operates at volt levels and must be interfaced to the millivolt-level signals of a superconducting processor. This has the advantage over superconducting circulating-current cells in that CMOS memory structures are very compact and are highly developed. Large memories can be made with high yield. CMOS works even better at 4 K, the usual operating temperature of niobium

superconducting circuits, than at 300 K, so it can be in close physical proximity to the processors. A block diagram of our memory with its interfacing circuits is shown in Fig. 1. The amplification of millivolt signals to volt-level signals at the input is accomplished by a two-stage amplifier. In our prior work, the first stage is a stack of Josephson junctions and the second stage is a hybrid amplifier comprising a MOS device with a large series array of Josephson junctions as its load. This is called the Ghoshal amplifier after its inventor [3]. The output currents from memory bit lines are detected by Josephson devices.

Results of research under this grant

We demonstrated in prior work [4] the access time for a single memory cell measured from the input few millivolt signal to the measured output from a bit line in 600 ps. Our goals for this present grant were to address some of the issues that will facilitate the completion of a 64-kbit hybrid Josephson-CMOS 4 K memory and to measure its access time and power dissipation. A completely new design for the CMOS memory was done by a professional memory designer. We incorporated design changes that allowed measurement of a complete word rather than a single bit. We also incorporated changes in the memory layout aimed at reduction or elimination of the troublesome electrostatic crosstalk between the clock and the millivolt-level output signals. This was done by incorporating grounded shielding lines around the output bit lines.

A major innovation was the introduction of a new input amplifier as an alternative to the Ghoshal amplifier used in our prior work, with the goals of higher speed and lower power dissipation. The function of the input amplifier is to raise the Josephson millivolt-level signals coming from the processor to the volt level need by the CMOS memory. This is optimally done using two stages as shown in Fig. 2. The first stage can be a Josephson based amplifier comprising two interconnected series arrays of Josephson junctions often called a Suzuki stack. The Ghoshal amplifier employs a Suzuki stack that produced an output of 40 mV when driven by an input of a few millivolts. The second stage is a hybrid of an MOS device with a load composed of 200 series-connected Josephson junctions. The new second-stage amplifier (Fig. 3) is based on a sensitive CMOS amplifier used in DRAM memories to detect bit line outputs. The threshold voltages in the constituent MOS devices have some statistical variations so the threshold for the amplifier has small random offsets. To assure robust switching it was necessary to require larger output from the first-stage Josephson circuits driving the second-stage CMOS amplifier. We devised a so-called superstack consisting of a series of four 8-junction Suzuki stacks, all being driven by the same inductively coupled input line as shown in Fig. 4. The superstack produces an 80 mV output .

Since the layout of the 64-kbit CMOS memory made in 180 nm technology has a footprint of only about 1 mm x 0.5 mm, it was possible to include two copies on the same 2.4 mm x 2.4 mm chip fabricated by TSMC through MOSIS. One copy is laid out to bump bond to a Josephson chip for the Ghoshal amplifier design and the other to bond to a different Josephson chip for the new amplifier design. The Josephson chips were made by HYPRES.

Testing of the 180 nm CMOS components during this grant period revealed that the almost infinite charge retention times measured earlier on 350 nm devices are not found on the advanced CMOS devices due to device leakage. Because of inadequate retention time, the leakage obviates the use of the 3T (or 4T) memory cells which we had incorporated. Also, it precludes use of a bias control circuit incorporated in the second stage of the Ghoshal amplifier. The leakage will be even worse in more advanced CMOS technology nodes such as 65 nm. This understanding has set the stage for the design of the next model in which we will have to use standard SRAM memory cells and a different approach to circuit bias.

References

[1] W. Anacker, "Potential of superconductive Josephson tunneling technology for ultrahigh performance memories and processors," *IEEE Trans. Magn*., Vol. MAG-5, pp. 968-975, December 1969.

[2] S. Nasagawa, H. Numata, Y. Hashimoto, and S. Tahara, “High-frequency clock operation of Josephson 256-word 16 bit RAMs,” *IEEE Trans. Appl. Superconduct*., Vol. 9, pp. 3708–3713, June 1999.

[3] U. Ghoshal, H. Kroger, and T. Van Duzer, “Superconductor-semiconductor memories,” *IEEE Trans. Appl.Supercond.*, Vol. 3, pp. 2315-2318, March 1993.

[4] K. Fujiwara, Q. Liu, T. Van Duzer, X. Meng, and N. Yoshikawa, “Half-Nanosecond Latency Measurement on a 64-kbit Josephson-CMOS Memory,” *IEEE Trans. Appl. Supercond*.. Vol. 20, pp. 14-20, Feb. 2010.

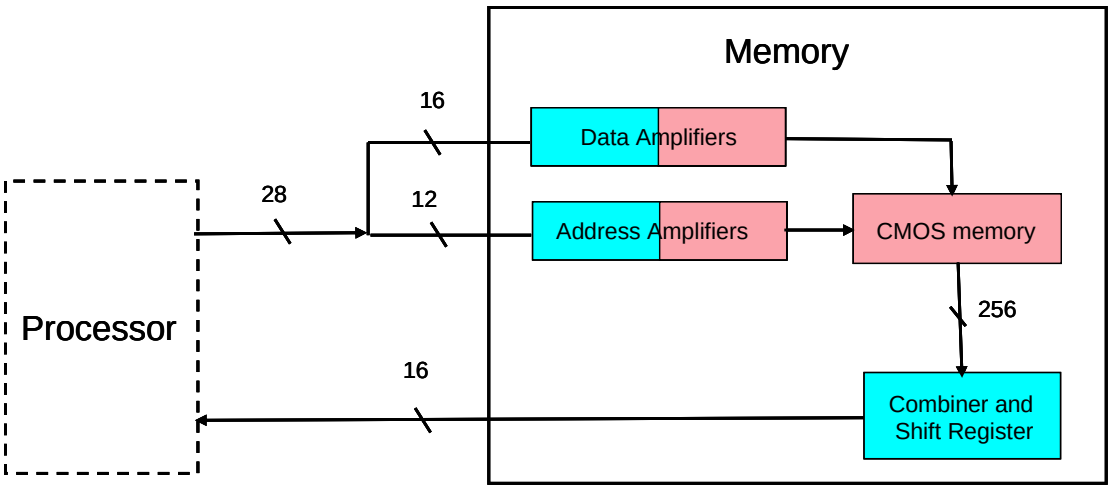

Fig. 1 Hybrid 4 K Josephson-CMOS 64 kb memory. The blue parts are made in Josephson technology and the pink parts are CMOS. The numbers on the lines show the numbers of lines in the buses.

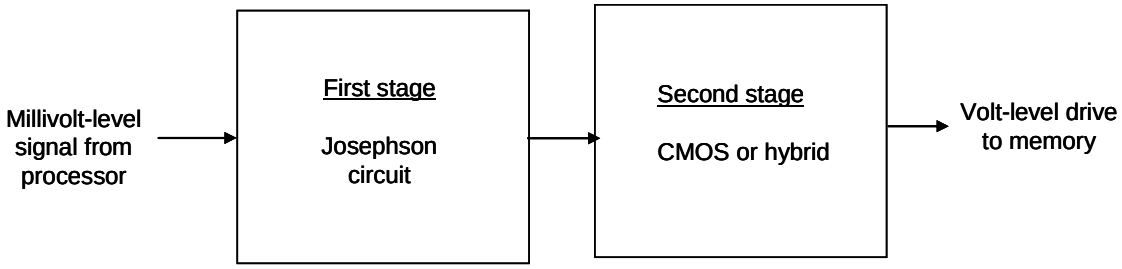

Fig. 2 Input amplifier, optimally made in two stages. The output from the first stage is several tens of millivolts.

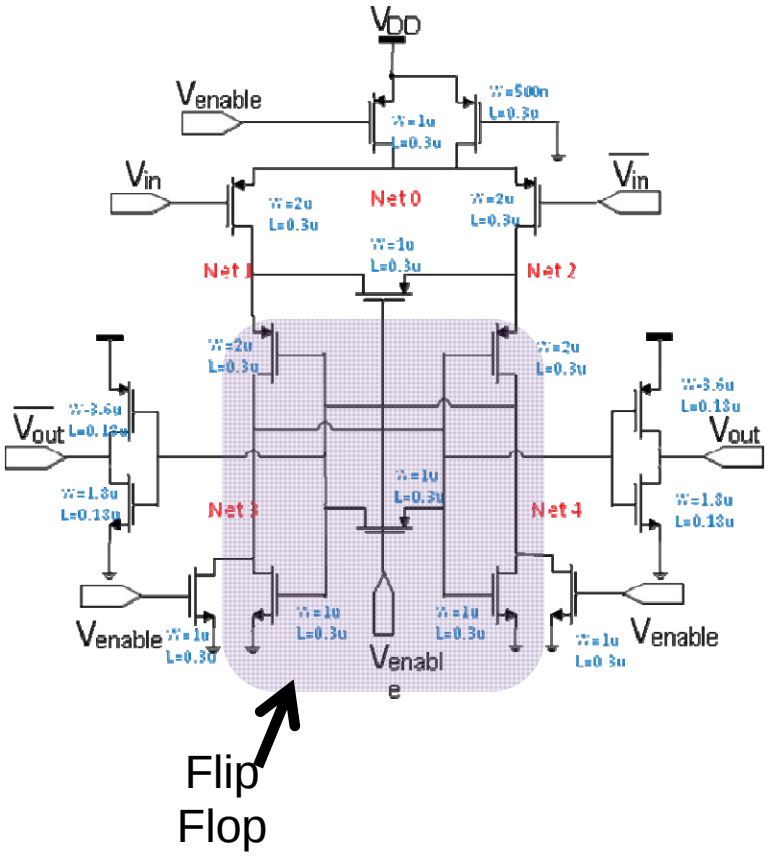

Fig. 3 CMOS latch amplifier as a choice for the second stage interface amplifier.

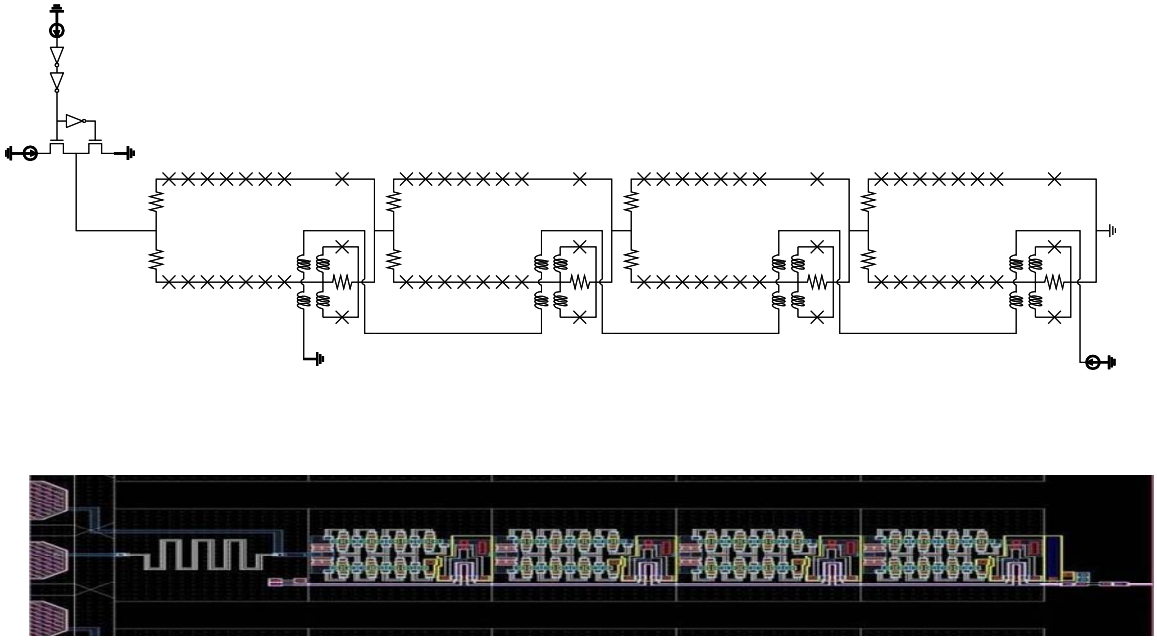

Fig. 4 Schematic and layout of a superstack comprising four 8-junction Suzuki stacks. (Resistor used in test for voltage supply to avoid need for CMOS components.)